

Nested Fast and Simultaneous Solution for Time-Domain Simulation of Integrative Power-Electric and Electronic Systems

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Abstract—As power electronics are increasingly used in power-electric networks, there is an interest in the creation of time-domain simulation techniques that can model the diversity of the integrative power-electric and electronic system while achieving high accuracy and computational speed. In the proposed method, generation of electric network equivalents (GENE), this is supported through the nested structure of the overall simulation process. One or multiple parent simulations, in which the unknown voltages are calculated using nodal analysis, launch multiple child simulations concerned with diakoptic subdivisions of the system under study. The interfaces for information exchange between parent and child levels are designed to provide encapsulation. This makes the subdivisions appearing from outside in the form of network branches compatible with the nodal analysis approach. It also facilitates the use of diverse solution methods for different child simulations, as it is shown for the simultaneous solution of equations formulated with nodal analysis and state space methods. Computational efficiency is obtained through the coordinated application of sparse-matrix methods, piecewise linear approximation of nonlinear characteristics, and precalculation of operations pertaining to recurring power-electronic switch statuses. The resulting overall solution process is simultaneous, distributed, and suitable for real-time simulation. The devised methodology is validated through simulation of the CIGRE HVdc benchmark model, comprising ac networks, twelve-pulse power-electronic converter stations, harmonic filters, and dc transmission.

Index Terms—Algorithms, circuit simulation, cosimulation, diakoptics, electromagnetic transients program (EMTP), HVdc transmission, modeling, numerical methods, parallel processing, power electronics, power system simulation, real-time systems, sparse-matrix techniques.

I. INTRODUCTION

AN important field of application for the simulators of the Electromagnetic Transients Program (EMTP) type [1] is the time-domain study of integrative power-electric and electronic systems. Examples of timely interest include simulations of storage and compensation systems [2], [3]; distributed generation (DG) [4], [5]; all-electric ship power systems; and high-voltage direct current (HVdc) systems [6]–[8]. The interfacing of the power-electronic converters and networks can be made through disconnection and prediction of the common

voltages and currents as shown in [6]. The time step must be small enough for the prediction to be accurate and to obtain numerical stability. Numerical stability can generally be enhanced by using an iterative scheme such as the compensation method [7] at the expense of an increased computational burden.

If no disconnections are made, then all couplings of lumped elements that exist in reality are retained in the models. This offers the possibility of designing a noniterative simultaneous solution [9] and is consistent with the objectives of this work. The method generation of electric network equivalents (GENE), proposed here, is centered on a noniterative simultaneous solution. It is to provide computational efficiency and accuracy while offering the flexibility of using locally diverse solution methods and retaining compatibility with existing simulation drivers based on nodal analysis, such as the EMTP. The computational efficiency envisaged is to be high enough to achieve at least real-time speed for the simulation of the CIGRE HVdc benchmark system on off-the-shelf PCs.

To avoid computationally expensive iterations, nonlinear device characteristics as those of power-electronic switches are here modeled through piecewise linear approximation as, for example, discussed in [10]. For the emulation of switching processes, methods for the fast noniterative simulation of switching, as described in [2], [11]–[13], are suitable. These methods have already been tested for real-time simulation.

To obtain an efficient simultaneous solution, different options have been considered. Popular schemes for the efficient simultaneous solution of a linear equation system $A\xi = b$ with the vector of unknown and dependent variables ξ are based on the exploitation of the given system topology that is mirrored through matrix A . The topology of many networks is such that the corresponding nodal admittance matrix contains a significant number of zero elements. Methods aimed at retaining this sparsity by reducing the number of nonzero fill-in elements generated in the factorized lower and upper triangular matrices obtained through LU factorization do exist. The minimum degree algorithm presented in [14] achieves this while considering the overall system as a single piece, hereafter referred to as a single-piece method. In conjunction, sparse-matrix structures that only store the nonzero elements are important [15].

As opposed to a single-piece method, tearing, also known as diakoptics, is a multipiece method that enables a simultaneous solution. One possible approach to tearing, the so-called node tearing [15], leads A to adopt the bordered block diagonal form as shown in Fig. 1, where symbol \subset indicates a subdivision. It is an advantage of this formulation that part of the local solutions

Manuscript received March 7, 2005; revised September 30, 2005. This work was supported by the National Science Foundation under Award ECS-0238523.

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Digital Object Identifier 10.1109/TPWRD.2006.876657

$$\begin{pmatrix} \mathbf{A}_{11} & \mathbf{A}_{12} \\ \mathbf{A}_{21} & \mathbf{A}_{22} \end{pmatrix} \begin{pmatrix} \xi_1 \\ \xi_2 \end{pmatrix} = \begin{pmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \end{pmatrix} \quad \mathbf{A}_{11} = \begin{pmatrix} \mathbf{A}_{111}^c & & \\ & \ddots & \\ & & \mathbf{A}_{11M^c}^c \end{pmatrix}$$

Fig. 1. From left to right: partitioned form of $\mathbf{A}\xi = \mathbf{b}$, blocks of \mathbf{A}_{11} along the diagonal.

corresponding to the M^c pieces of subdivisions of \mathbf{A}_{11} may be calculated in parallel. Then, the connections between the subdivisions through border matrices \mathbf{A}_{12} , \mathbf{A}_{21} , and \mathbf{A}_{22} are taken into account to get the overall solution. Of particular interest is the intersection network equation $\mathbf{A}^\cap \xi_2 = \mathbf{b}^\cap$, here marked with \cap to signify intersection

$$\mathbf{A}^\cap = \mathbf{A}_{22} - \mathbf{A}_{21} \mathbf{A}_{11}^{-1} \mathbf{A}_{12} \quad (1)$$

$$\mathbf{b}^\cap = \mathbf{b}_2 - \mathbf{A}_{21} \mathbf{A}_{11}^{-1} \mathbf{b}_1. \quad (2)$$

The intersection network is an accurate miniature equivalent of the original network. The number of unknowns is so reduced to ξ_2 , i.e., the unknowns of the intersection network that interconnects the subdivisions. These unknowns are therefore incident at the terminals of the subdivisions.

Multipiece and single-piece methods can be combined, for example, by first creating the bordered block diagonal form of a matrix and then considering the blocks as single pieces to which the minimum degree algorithm is applied [14].

The nested parent-child simulation method GENE presented in this work makes use of combined multi and single-piece solutions as well as sparse-matrix storage structures. In GENE, the intersection network, which is dealt with by the parent simulation, is not obtained using (1) and (2). Instead, miniature equivalents of subdivisions of power-electric network parts and power-electronic converters are calculated using Norton's theorem in a first step. The obtained miniature equivalents are then interconnected at their terminal nodes to obtain the intersection network. The proposed method is particularly well suited as the basis of techniques for fast and simultaneous simulation of integrative power-electric and electronic systems where diverse behavior is observed.

To provide the reader with a relevant background and basis of comparison, selected foundations of transients simulation based on nodal analysis are elaborated upon in Section II. In Section III, the concept of the nested parent-child simulation is developed for nodal analysis techniques. The formulation is extended in Section IV to show the capability of simultaneous cosimulation based on both nodal analysis and state-space methods. The application and validation tests in Section V are centered on the CIGRE HVdc Benchmark model and show that accurate simulation at speeds faster than real time is achieved on an off-the-shelf PC. Conclusions are drawn in Section VI. In Appendices A and B, the application of the weight-averaged integration method for the purpose of modeling network branches and discretizing dynamic state equations is explained, respectively. In Appendix C, details of the algorithms of the nested parent-child simulation are elaborated upon.

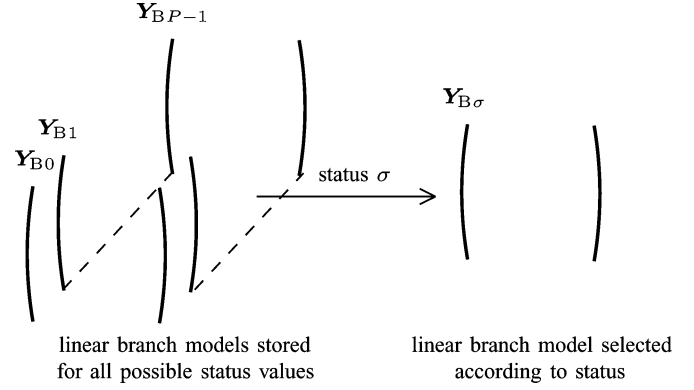


Fig. 2. Access to branch admittance matrices corresponding to piecewise linear approximation.

II. BASICS OF BRANCH AND NETWORK MODELING FOR TIME-DOMAIN TRANSIENTS SIMULATION

In order to obtain the network model for time-domain transients simulation based on nodal analysis, models of the branches that make up the network need to be available. Using the concept of companion modeling, the branches are described in the following form:

$$\mathbf{Y}_B \mathbf{v}_B = \mathbf{j}_B + \mathbf{i}_B \quad (3)$$

where \mathbf{Y}_B is the nodal admittance matrix of the branch; \mathbf{j}_B is the vector of the source-dependent nodal current injections that are updated at each time step in accordance with changing initial conditions of the difference equations; \mathbf{v}_B is the vector of the nodal voltages of the branch; and \mathbf{i}_B is the vector of the currents flowing into the branch. The derivation of (3) is detailed in Appendix A.

Using the piecewise linear approximation of the nonlinear characteristic of a power semiconductor valve in [10], two statuses corresponding to two distinct companion models distinguish between conducting and blocking modes. In general, P segments of straight lines may be used to approximate a non-linear function. Then, \mathbf{Y}_B is obtained from a tensor comprising information for P distinct branch companion models. To build up the network model, the one branch model that corresponds to the active status σ is selected as indicated in Fig. 2. Changes of status involve modifications of \mathbf{Y}_B and \mathbf{j}_B in (3).

The network model is obtained through direct construction [16], also referred to as stamping. First, all branches are conceptually removed from the network and then added successively in order to add the entries of \mathbf{Y}_B to the emerging nodal admittance matrix in accordance with the network topology. The equation system for the network model is then partitioned to distinguish between the voltages \mathbf{v}_d that are unknown and dependent and the voltages \mathbf{v}_e that are known and given through excitation functions

$$\begin{pmatrix} \mathbf{Y}_{dd} & \mathbf{Y}_{de} \\ \mathbf{Y}_{ed} & \mathbf{Y}_{ee} \end{pmatrix} \begin{pmatrix} \mathbf{v}_d \\ \mathbf{v}_e \end{pmatrix} = \begin{pmatrix} \mathbf{j}_d \\ \mathbf{j}_e + \mathbf{i}_e \end{pmatrix} \quad (4)$$

where \mathbf{j}_d , \mathbf{j}_e are, respectively, the source-dependent nodal current injections into the nodes with unknown and known voltages

and \mathbf{i}_e are the currents that flow through the nodes with known voltages.

Given that there are N unknown voltages, the $N \times N$ matrix \mathbf{Y}_{dd} is factorized into lower and upper triangular matrices $\mathbf{Y}_{dd} = \mathbf{L}_{dd}\mathbf{U}_{dd}$. The unknowns are obtained through the forward and backward substitution [17] by solving the following equation derived from the first row of (4):

$$\mathbf{L}_{dd}\mathbf{U}_{dd}\mathbf{v}_d = \mathbf{j}_d - \mathbf{Y}_{de}\mathbf{v}_e. \quad (5)$$

III. NODAL-ANALYSIS-BASED SIMULATION WITH GENE

While the nested parent–child simulation method GENE supports the use of diverse solution methods, its parent simulation as the driver of the overall solution process uses nodal analysis. In Section III-A, the parent simulation is described. Before the child simulations are explained, it needs to be shown how the child subdivisions are defined and their miniature equivalents are obtained. This is done in Sections III-B and III-C, respectively. The status indicator and access scheme for precalculation and storage at the child simulation level and the child simulation process itself are then developed in, respectively, Sections III-D and III-E. An analytic evaluation of the improvement in efficiency provided by the status indicator and access scheme is proposed in Section III-F. Details of the developed algorithms are discussed in Appendix C.

A. Parent Simulation

As mentioned in Section II, the stamping method is widely used to build up the network model using the given branch models. At the parent simulation level, however, the stamping is applied to entire child subdivisions rather than individual branches. Prior to the stamping action, child subdivisions, as the one shown in Fig. 3, are reduced to miniature equivalents where only the terminal nodes at the boundaries of the subdivisions remain. As detailed in subsequent Sections III-B and III-C, this is done in order to have the child subdivision appear in the format of branch companion models

$$\mathbf{Y}_N^c \mathbf{v}_t^c = \mathbf{j}_N^c + \mathbf{i}_t^c \quad (6)$$

where \mathbf{Y}_N^c is the nodal admittance matrix of the miniature equivalent of the child subdivision; \mathbf{j}_N^c is the vector of the source-dependent nodal current injections into the terminal nodes of the child subdivision; \mathbf{v}_t^c is the vector of the nodal voltages at the terminal nodes; \mathbf{i}_t^c is the vector of the currents flowing into the child subdivision. Equation (6) is indeed of the same format as (3). It is this analogy, to be detailed in Section III-C, that enables the use of the stamping method for the construction of the network model in exactly the same way for companion models of simple branches as well as for miniature equivalents of entire power-electronic converters and electric network parts. Since the stamping is applied to the miniature equivalents (6), the only unknown voltages to be solved for at the parent simulation level are those at the terminals of the child subdivisions.

The main steps of the parent simulation level are detailed in the pseudocode of Fig. 4. All terminal voltages are calculated in

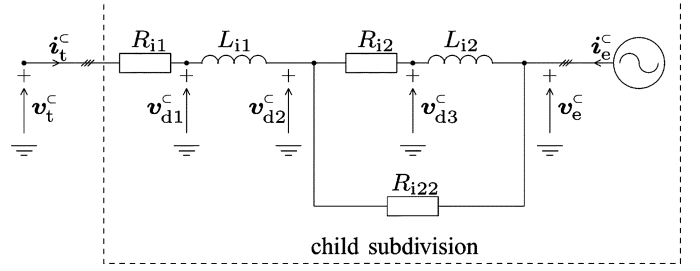


Fig. 3. AC network on the inverter side of the CIGRE HVdc benchmark model represented as a child subdivision.

- Step 1: Calculate nodal voltages: $\mathbf{Y}_{dd}^n \mathbf{v}_d^n = \mathbf{j}_d^n - \mathbf{Y}_{de}^n \mathbf{v}_e^n$.
- Step 2: For all child subdivisions do: perform child simulations.
- Step 3: If there is a status change of the network, then do:
 - Step 3.1: Reconstruct \mathbf{Y}_{dd}^n accordingly.
 - Step 3.2: Refactorize \mathbf{Y}_{dd}^n into \mathbf{L}_{dd}^n and \mathbf{U}_{dd}^n .
- Step 4: Advance the time dependent excitation sources of the network.
- Step 5: According to the sources and status of the network construct \mathbf{j}_d^n .
- Step 6: Increment time step counter. If termination condition is met, then exit. Else return to step 1.

Fig. 4. Course of actions in parent simulation using GENE.

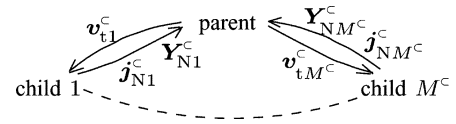


Fig. 5. Information exchange between parent and child simulations.

step 1. The symbol for intersection \cap is used to stress that the ensemble of all unknown terminal voltages of child subdivisions makes up the vector of unknown voltages of the intersection network. Then, the child simulations are called in step 2. Thus, the parent simulation launches new child simulations, leading to a nested structure. The information exchange between parent and M^c different child simulations is clarified in Fig. 5. At the beginning of step 2, the child simulations receive their respective terminal voltages as inputs. These terminal nodes are, of course, incident at the intersection network and, therefore, known from step 1. At the end of step 2, the subdivisions return their respective miniature equivalents to the parent simulation process.

If any of the returned \mathbf{Y}_N^c has been modified, for example, due to a change of status of a piecewise linear approximation, then in step 3.1, matrices are reconstructed using stamping in accordance with the updated status of the network. Furthermore, the LU factorization is performed in step 3.2. In step 4, the time-dependent excitation sources are advanced. In step 5, the vector of the source-dependent nodal current injections \mathbf{j}_d^n is constructed. In step 6, the time step counter is incremented and the termination condition is checked. The loop is entered again at step 1 if the termination condition is not met.

For the purpose of comparison, step 2 is shown in Fig. 6 in a simulation process without nesting. As a comparison with Fig. 4 shows, branches are dealt with analogous to child subdivisions. It is important to note that all remaining steps can be retained as in Fig. 4. This analogy of simulator design ensures compatibility of the nested simulation with existing simulation drivers based on nodal analysis.

Step 2: For all branch models do: perform branch simulations.

Fig. 6. Step 2 in simulation without further nesting.

While the pseudocode in Fig. 4 gives the basic outline of the parent simulation, selected techniques have been added to increase accuracy and computational speed. Especially when power electronics are to be simulated in real time, it is important to track switching events accurately and efficiently, and this can be done here as described in [11].

If the network contains transmission paths for which the wave traveling times between both ends are equal to or larger than the time step size, then both ends are isolated mathematically for at least one time step interval [18]. For each portion, a separate nodal admittance matrix can be established.

B. Child Subdivision

As an example of realizing a child subdivision, the three-phase ac network on the inverter side of the CIGRE HVdc benchmark system, shown in Fig. 3, is considered. The excitation voltages \mathbf{v}_e^C are given by the three-phase voltage source. Voltages \mathbf{v}_{d1}^C , \mathbf{v}_{d2}^C , and \mathbf{v}_{d3}^C are dependent and unknown. Terminal voltages \mathbf{v}_t^C appear as inputs coming from the parent simulation. When all inductors are replaced by their companion models as shown in Appendix A and stamping is applied, child subdivisions can be described in the following general form:

$$\begin{pmatrix} \mathbf{Y}_{dd}^C & \mathbf{Y}_{de}^C & \mathbf{Y}_{dt}^C \\ \mathbf{Y}_{ed}^C & \mathbf{Y}_{ee}^C & \mathbf{Y}_{et}^C \\ \mathbf{Y}_{td}^C & \mathbf{Y}_{te}^C & \mathbf{Y}_{tt}^C \end{pmatrix} \begin{pmatrix} \mathbf{v}_d^C \\ \mathbf{v}_e^C \\ \mathbf{v}_t^C \end{pmatrix} = \begin{pmatrix} \mathbf{j}_d^C \\ \mathbf{j}_e^C + \mathbf{i}_e^C \\ \mathbf{j}_t^C + \mathbf{i}_t^C \end{pmatrix}. \quad (7)$$

In the case of the example, vector \mathbf{v}_d^C then comprises three three-phase voltages $\mathbf{v}_d^C = (\mathbf{v}_{d1}^C \ \mathbf{v}_{d2}^C \ \mathbf{v}_{d3}^C)^T$.

The creation of child subdivisions in the format described allows for encapsulation. This means that all computations that concern a child subdivision are performed locally within the child simulation process. In order to perform forward and backward substitutions locally, \mathbf{Y}_{dd}^C is factorized into lower and upper triangular matrices \mathbf{L}_{dd}^C and \mathbf{U}_{dd}^C . Based on the first row of (7), \mathbf{v}_d^C is then calculated with the following equation:

$$\mathbf{L}_{dd}^C \mathbf{U}_{dd}^C \mathbf{v}_d^C = \mathbf{j}_d^C - \mathbf{Y}_{de}^C \mathbf{v}_e^C - \mathbf{Y}_{dt}^C \mathbf{v}_t^C. \quad (8)$$

In order to boost the efficiency at the child simulation level, the minimum degree algorithm and sparse-matrix storage structures, as discussed in Section I, are applied.

C. Contractual Interfacing Through Companion Model Emulation

In order to obtain the companion model of a miniature equivalent of a child subdivision given through (6), \mathbf{v}_d^C is eliminated in (7) using the Kron reduction formula [19]. The miniature equivalents of the nodal admittance matrix and source vector then constitute Norton equivalents in the form given through (3). A comparison of (3) and (6) shows that vector \mathbf{v}_t^C corresponds to \mathbf{v}_B^C , and \mathbf{Y}_N^C and \mathbf{j}_N^C , respectively, correspond to \mathbf{Y}_B^C and \mathbf{j}_B^C . As already indicated in Section III-A, interfacing parent and child simulations through companion models allows

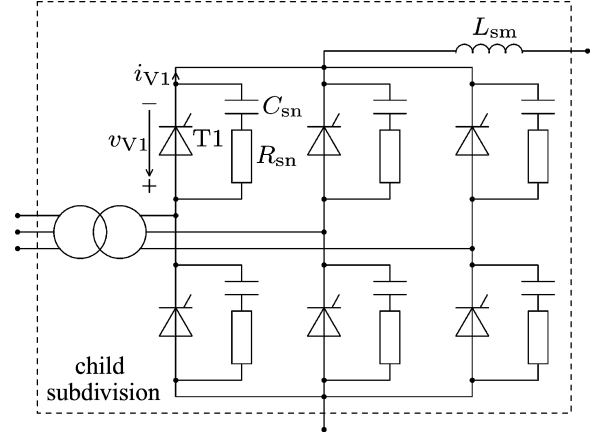


Fig. 7. Power-electronics converter represented as a child subdivision.

for the use of the stamping method. This interfacing involves no disconnection so that couplings between multiple subdivisions are retained as in reality. An intersection network description analogous to the one of (1) and (2) is therefore directly obtained through stamping. Further details on the calculation of the Norton equivalent are given in Appendix C.1.

D. Subdivision Status Indicator and Access Scheme

As justified and mentioned in Sections I and II, piecewise linear approximation is used here to model nonlinear characteristics of branches. Since statuses are associated with branches as shown in Fig. 2, statuses must also be associated with child subdivisions. This is because the miniature equivalents adopt the same format as branch companion models. Through the status indicator scheme, a subdivision status variable s is associated with each possible combination of status values of piecewise linear approximations in a subdivision. Details of the algorithms involved in the status indicator and access scheme are given in Appendix C.2.

Consider the child subdivision in Fig. 7, where, for the purpose of this example, the nonlinearities of the thyristors and saturable smoothing inductor L_{sm} are studied. If the thyristor is represented through two statuses and the smoothing inductor saturation characteristic is represented through three statuses, then the total number of possible statuses of this child subdivision with six thyristors and one smoothing inductor is $S = 2^6 \cdot 3^1 = 192$.

Child subdivisions can be defined in very different ways as the comparison of Figs. 3 and 7 shows. The subdivision status indicator and access scheme is flexible in that it can be applied to any of them and is not confined to any preselected type of circuit. The particular selection of the child subdivision boundaries as shown in Fig. 7 mirrors the definition of an HVdc object model for fast simulation presented in [8]. A twelve-pulse HVdc converter station can so be modeled by the connection of two six-pulse arrangements for each of which in the example 192 different statuses do exist. In general, for subdivision m , there are S_m different statuses, and information is stored for each status. Given that there are M^C child simulation processes, there are $\sum_{m=1}^{M^C} S_m$ different statuses for which information is stored at the child simulation level. At the parent simulation

level, there are $\prod_{m=1}^{M^C} S_m$ statuses because with each subdivision added, the number of different statuses is multiplied by S_m . Since $\sum_{m=1}^{M^C} S_m$ can be made much lower than $\prod_{m=1}^{M^C} S_m$, tearing into subdivisions and considering status values at the child simulation level can reduce storage requirements significantly. In the example of the twelve-pulse HVdc converter station, this becomes obvious since $192 + 192 \ll 192 \cdot 192$.

Before the simulation starts, matrices associated with a child subdivision, such as the miniature equivalent matrix \mathbf{Y}_N^C , are calculated and stored in a sparse-matrix storage structure [15] in fast accessible memory for each status s of a subdivision. The memory addresses showing where the matrices can be accessed are stored in an array [20]. Access to the matrices is then possible in the same way as described in Fig. 2. However, rather than accessing branches of status σ , child subdivisions of status s are accessed.

E. Child Simulation Process

As shown in Fig. 5, the child simulation receives the terminal voltages as input. It uses this information to calculate the nodal voltages within the child subdivision using (8). It performs further steps to return the Norton source as detailed in the pseudocode developed in Appendix C.3. The use of the subdivision status indicator and access scheme allows the avoidance of refactorizations. Thanks to the contractual interfacing through branch emulation, the overall solution process is simultaneous.

F. Efficiency Contributions of Subdivision Status Indicator and Access Scheme

In order to obtain an efficient overall simulation process, suitable intersection and subdivision networks to associate with the parent and child simulation processes are selected. In particular, when using parallel processing, it is advantageous to keep the computational effort for the different child simulation processes at a similar level by defining subdivisions of similar complexity. Reductions in storage requirement are usually achieved by reducing the number of status values per subdivision as discussed in Section III-D. At the same time, it is desirable to keep the size of the intersection network small to obtain a fast parent simulation process. General guidelines and further discussions on the network tearing are, for example, given in [15], [21]–[23].

As the multiplication count performed in Appendix C.4 demonstrates, the computational speed of GENE exceeds the one that is obtained when just using node tearing. This speedup is attributed to the subdivision status indicator and access scheme. When status changes occur, costly refactorizations do not need to be performed at the child simulation level. For the same reason, in GENE, the multiplication count does not change with status changes but remains constant. This makes the method suitable for real-time applications where a constant computational burden at any time step is desired.

IV. SIMULTANEOUS COSIMULATION WITH GENE

A feature of GENE is the ability to integrate diverse solution techniques within a simultaneous overall simulation process.

A. Concept

The child simulation uses the input information \mathbf{v}_t^C in order to calculate and return $\mathbf{Y}_N^C, \mathbf{j}_N^C$ as output. Due to the encapsulation property, the implementation of these calculations is hidden. The use of diverse solution methods in different child simulation processes is therefore supported. This is useful if models of subdivisions are available in a format not based on nodal analysis. As long as the presented rules for contractual interfacing described in Section III-C are respected, simultaneous cosimulation is obtained.

B. Case Study: Cosimulation With State-Space Methods

The state-space method and associated dynamic state equations provide a well-established framework [24] for the modeling of dynamic systems.

1) *Child Subdivision*: For the purpose of illustrating the simultaneous cosimulation of nodal and dynamic state equations, a linear lumped passive circuit is modeled with dynamic state equations and brought into a format that allows for use in a child simulation

$$\begin{pmatrix} \mathbf{A}^C & \mathbf{B}^C \\ \mathbf{C}^C & \mathbf{D}^C \end{pmatrix} \begin{pmatrix} \mathbf{x}^C \\ \mathbf{v}_t^C \end{pmatrix} = \begin{pmatrix} \dot{\mathbf{x}}^C \\ \mathbf{i}_t^C \end{pmatrix} \quad (9)$$

where the newly introduced symbol \mathbf{x} refers to the vector of dynamic state variables. Using weight-averaged integration, (9) can be discretized as shown in detail in Appendix B. The result is the model of the child subdivision

$$\begin{pmatrix} \mathbf{P}^C & \mathbf{Q}^C \\ \mathbf{C}^C & \mathbf{D}^C \end{pmatrix} \begin{pmatrix} \mathbf{x}^C \\ \mathbf{v}_t^C \end{pmatrix} = \begin{pmatrix} \boldsymbol{\eta}_x^C \\ \mathbf{i}_t^C \end{pmatrix} \quad (10)$$

where $\boldsymbol{\eta}_x^C$ only depends on results from previous time steps as shown in Appendix B. Once \mathbf{v}_t^C is obtained at the beginning of step 2 from the parent simulation, the state variables can be calculated as

$$\mathbf{L}_P^C \mathbf{U}_P^C \mathbf{x}^C = \boldsymbol{\eta}_x^C - \mathbf{Q}^C \mathbf{v}_t^C \quad (11)$$

where

$$\mathbf{P}^C = \mathbf{L}_P^C \mathbf{U}_P^C. \quad (12)$$

2) *Contractual Interfacing Through Companion Model Emulation*: Equation (10) is already brought into a form to provide the possibility of contractual interfacing through companion model emulation. To obtain the miniature equivalent of (6), the first row of (10) is eliminated using Kron's reduction

$$\mathbf{Y}_N^C = \mathbf{D}^C - \mathbf{T}_{CP}^C \mathbf{Q}^C \quad (13)$$

$$\mathbf{j}_N^C = -\mathbf{T}_{CP}^C \boldsymbol{\eta}_x^C \quad (14)$$

and the transfer matrix \mathbf{T}_{CP}^C

$$\mathbf{T}_{CP}^C \mathbf{P}^C = \mathbf{C}^C. \quad (15)$$

The elements of \mathbf{T}_{CP}^C are obtained using forward and backsubstitutions. Equations (13)–(15) define the companion model of

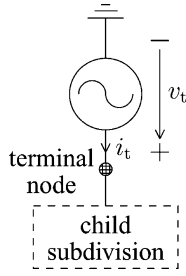


Fig. 8. Test circuit for evaluation of the child subdivision.

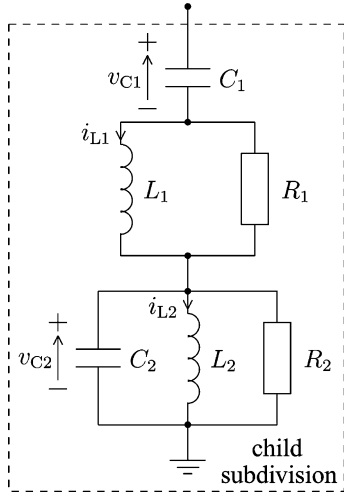


Fig. 9. Fourth-order highpass ac filter.

(6) to be stamped into the parent simulation process with the information exchange of Fig. 5.

V. APPLICATION AND VALIDATION

The nested parent-child simulation method GENE was implemented in the simulator virtual integrator for synthesis, testing, and analysis (VISTA). Two studies are presented for the purpose of validating the performance of the nested parent-child simulation. In the first study, a harmonic filter is represented in the form of a child subdivision. Then, the CIGRE HVdc benchmark model is implemented.

A. Lumped Linear Circuit

This validation test is aimed at verifying the methodology when a child simulation process is formulated based on the state-space method while nodal analysis is used for the parent simulation. For the validation test, the terminal voltage v_t is applied through an ideal voltage source as shown in Fig. 8. The considered lumped linear circuit in the subdivision is the fourth-order highpass ac filter of the CIGRE HVdc benchmark model and is shown in Fig. 9. The dynamic state variables are the currents through the inductors and the voltages across the capacitors $\mathbf{x}^c = (i_{L1} \ i_{L2} \ v_{C1} \ v_{C2})^T$. The parameters are as follows:

$$\begin{aligned} R_1 &= 83.00 \ \Omega, & R_2 &= 50.00 \ \Omega, & L_1 &= 15.10 \ \text{mH}, \\ L_2 &= 9.69 \ \text{mH}, & C_1 &= 6.57 \ \mu\text{F}, & C_2 &= 78.90 \ \mu\text{F}. \end{aligned}$$

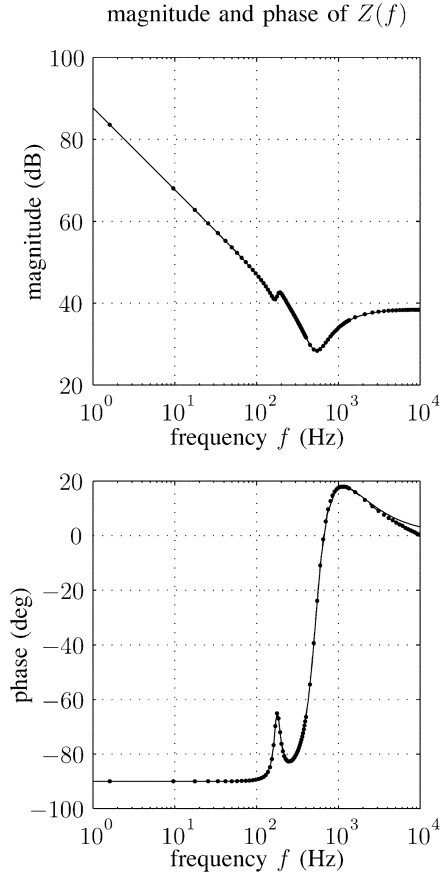


Fig. 10. Bode diagram for the fourth-order highpass filter; exact —, simulated with method GENE ●—.

The time step size of the simulation is equal to $50 \ \mu\text{s}$ and, in the weight-averaged method discussed in Appendix B, $w = 1$ is selected to obtain the trapezoidal method because it is very well suited for simulating the sinusoidal waveforms.

The bode diagram of the impedance Z of the harmonic filter measured at different source frequencies is depicted in Fig. 10. As a reference, the exact solution is drawn in the same diagram. The agreement of the measured and exact curves is clearly recognizable and confirms the high degree of accuracy of the simulation process. The deviation observed at very high frequencies is caused by the numerical integration.

B. CIGRE HVDC Benchmark Model

The CIGRE HVdc benchmark model [25], shown in Fig. 11, is a well-accepted testbed for simulation.

1) *Decomposition Into Parent and Child Simulations*: Modeling the wave propagation of the dc line using distributed parameters and its losses through lumped elements, the model can be partitioned into two portions assigned to parents A and B. Each parent simulation calls five child simulations to simulate the child subdivisions. Subdivisions A.4 and A.5 are defined in accordance with suggestions in [8]. Valves are modeled with a snubber $R_{sn} = 6000 \ \Omega$, $C_{sn} = 40 \ \text{nF}$ as shown in Fig. 7. The valve modeling technique described in [10] is applied. With one three-phase node counted as three single-phase nodes, the interconnection network of the parent simulation in portion A has only

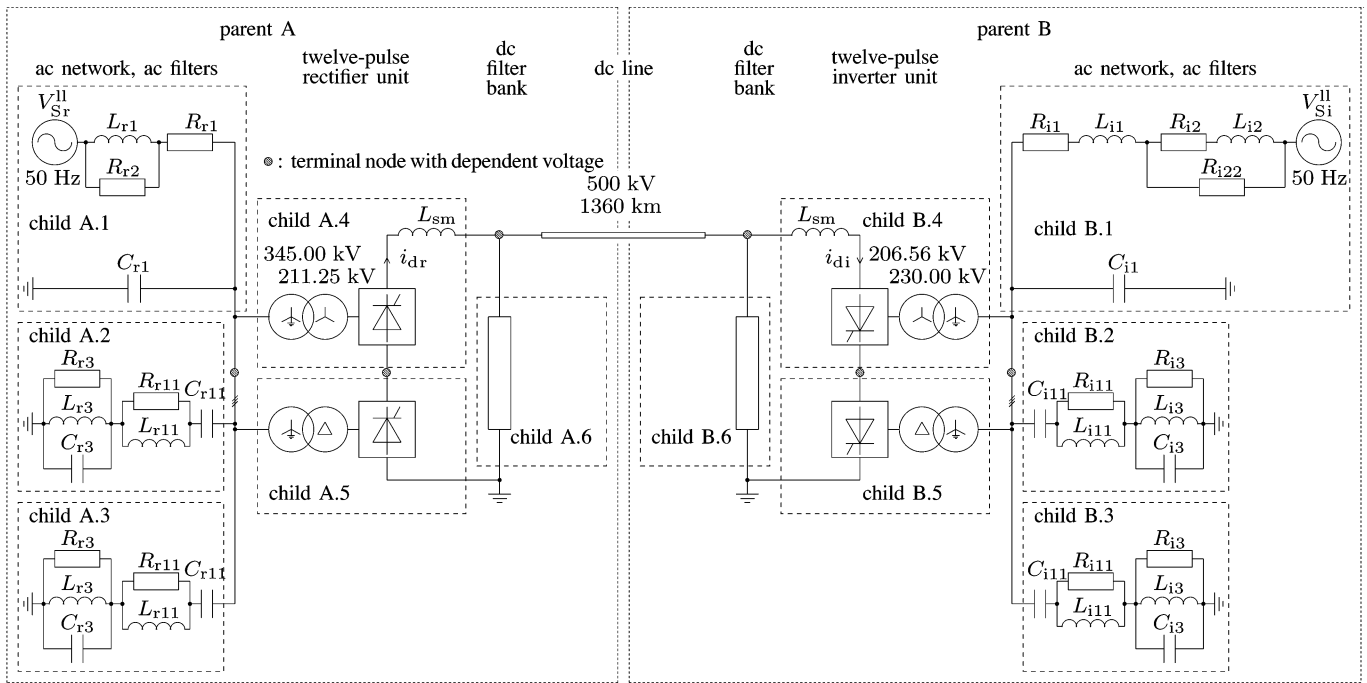


Fig. 11. CIGRE HVdc benchmark model.

five single-phase nodes. Portion B, the inverter side, is dealt with in the same way as portion A.

2) *Compilation and Hardware:* The program for the execution was generated by means of the compiler and linker DJGPP, version 2. The hardware comprises one processor Intel Pentium 4 2.4 GHz and a random-access memory (RAM) of 256 MB.

3) *Waveform Comparison:* The simulations of the valve voltage v_{V1} and valve current i_{V1} marked in Fig. 7 are depicted in Fig. 12. The results obtained with a simultaneous solution using the DCG EPRI Version 3.a of the EMTp at a time step of $10 \mu s$ are depicted on the left. The results obtained with GENE at a time step size of $100 \mu s$ are shown on the right. In the used EMTp version, a method to pinpoint switching events through interpolation is not available. In the GENE simulation, switching events were tracked as discussed in [11]. Therefore, a much larger time step size could be selected for the method GENE.

The results show very close agreement and are in accordance with the commutation processes observed in HVdc converter stations. In general, it can be said that the observed accuracy matches that obtained with simultaneous single-piece solutions where comparable methods for the representation of nonlinearities are employed. This is plausible because the process of generating miniature equivalents of the child subdivision does not involve further approximations, and the nested multipiece solution is simultaneous.

4) *Time Comparison:* Applying the method GENE as a nested simulation, the largest measured computation time for the execution of all calculations per time step was of the order of $30 \mu s$. Real-time or faster-than-real-time speed can be achieved on an off-the-shelf PC with one processor when selecting a time step size larger than $30 \mu s$. In Table I, this time is compared with results obtained using alternative solutions.

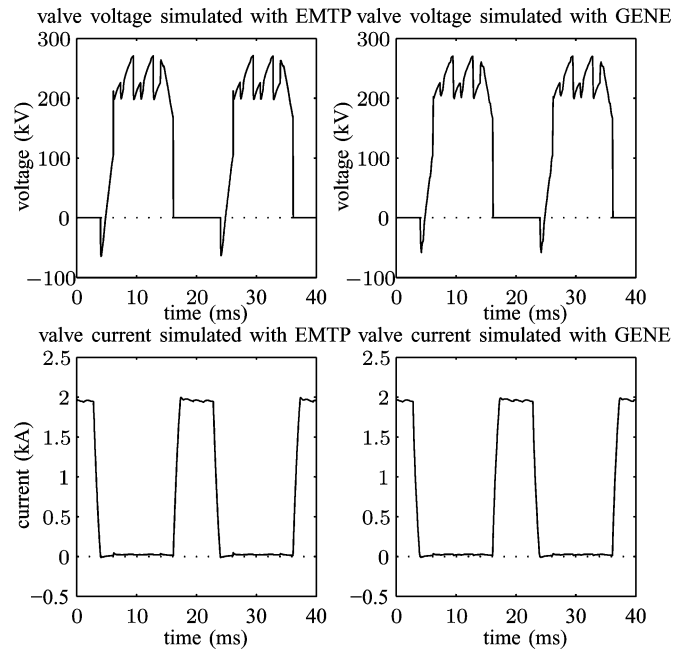


Fig. 12. Valve voltages and currents of the CIGRE HVdc benchmark model.

Applying the minimum degree algorithm to each of the parent simulations separately and considering each of the two associated networks as a single piece, the time obtained is $39 \mu s$. In the full-matrix solution, no such optimizations are applied. The results confirm the computational efficiency of the nested parent-child simulation.

The method GENE, as a combination of multipiece and single-piece methods, simulated the benchmark faster than the single-piece method alone. This performance shows that

TABLE I
MAXIMAL COMPUTATION TIMES PER TIME STEP

GENE	minimum degree	full-matrix
30 μ s	39 μ s	300 μ s

the methodology of reducing the size of the matrix to where refactorization is applied at the parent simulation level and then using the minimum degree method, precalculation, and storage at the child simulation level is effective.

Parallel processing of multiple child simulation processes can further improve the computation time although this requires multiple processors. With the single-processor hardware as mentioned in Section V-B2, parallel processing cannot be performed. Together with the cosimulation capability, the possibility to run fast simulation appears here as one of the main advantages of GENE. Speeds faster than real time are achieved with a single processor for the CIGRE HVdc benchmark system.

VI. CONCLUSION

The method GENE as a nested solution for the time-domain simulation of transients of integrative power-electric and electronic systems was proposed, implemented, and tested. The overall solution process is decomposed hierarchically into parent and child simulations. The parent simulation calculates the voltages at the terminal nodes of the child subdivisions. In the child simulations, the local voltages at the nodes within the subdivisions are calculated. The proposed interfacing between parent and child simulations through companion model emulation is clearly defined and organized in that child subdivisions are treated in the same way as companion models of branches. This enables compatibility with existing simulation drivers based on nodal analysis. Furthermore, the calculations within the child simulations are encapsulated and the application of locally different solution procedures is so supported. This was demonstrated through a simultaneous cosimulation involving both the nodal analysis and state-space methods.

A subdivision status indicator and access scheme was devised in order to avoid refactorizations at the child simulation level and, thus, enhance computational speed. For each status, a set of sparse matrices and vectors is precalculated and prestored, retaining the sparsity so that the corresponding information is readily available during the simulation. It requires that nonlinear characteristics inside a child subdivision be modeled by means of piecewise linear approximation. The application of the status indicator and access scheme is of particular interest in real-time simulation as the computational burden is well balanced over successive time step intervals.

The boundaries of the child subdivisions are selected manually by the user. An idea for future work is to devise an algorithm that automatically decomposes the overall system into child subdivisions. The objective function of the algorithm would aim to minimize the overall computational effort. In this context, the multiplication count formulas presented in this paper constitute an important step towards the evaluation of the computational effort.

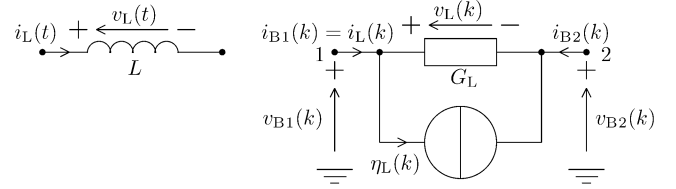


Fig. 13. Conventions for inductor: Left: description in continuous time domain. Right: companion branch model in discrete time domain.

In conjunction with a method for the tracking of switching events, the GENE method was implemented in the simulator virtual infrastructure for synthesis, testing, and analysis (VISTA) and tested through the simulation of the CIGRE HVdc benchmark model. The simultaneous nested solution has shown to give the same level of accuracy as a simultaneous single-piece solution. The nested solution has shown to be faster than the single-piece solution. Faster than real-time performance was achieved on a standard PC. The combination of computational efficiency and accuracy at any time step, the flexibility of using locally diverse solutions, and the compatibility with existing simulation drivers based on nodal analysis make the method so well suited for time-critical transients simulation of the diverse combination of power-electric and electronic systems.

APPENDIX

A. Companion Branch Modeling With Weight-Averaged Integration

The differential equations describing individual network branches are approximated by means of numerical integration. For example, the behavior of the inductor in Fig. 13 is described through the following differential equation:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L}. \quad (\text{A.1})$$

Using weight-averaged integration with time step size τ , (A.1) is discretized

$$i_L(k) = \frac{\tau(2-w)}{2L}v_L(k) + i_L(k-1) + \frac{\tau w}{2L}v_L(k-1). \quad (\text{A.2})$$

For $w = 1$, the trapezoidal method and for $w = 0$, the backward-Euler method are obtained as discussed in [12]. By substituting

$$G_L = \frac{\tau(2-w)}{2L}, \quad \eta_L(k) = i_L(k-1) + \frac{\tau w}{2L}v_L(k-1)$$

the inductor is modeled through a companion model as shown on the right-hand side of Fig. 13. By setting $\mathbf{i}_B = (i_{B1} \ i_{B2})^T$, $\mathbf{v}_B = (v_{B1} \ v_{B2})^T$ and using the conventions indicated in Fig. 13, \mathbf{Y}_B and \mathbf{j}_B of (3) can be determined for the inductor example

$$\mathbf{Y}_B = \begin{pmatrix} G_L & -G_L \\ -G_L & G_L \end{pmatrix}, \quad \mathbf{j}_B = \begin{pmatrix} -\eta_L(k) \\ \eta_L(k) \end{pmatrix}. \quad (\text{A.3})$$

B. Discretization of Dynamic State Equations With Weight-Averaged Integration

Using the weight-averaged method for flexible integration as in Appendix A, the differential equation in the first row of (9) is discretized

$$\frac{2-w}{2} (\mathbf{A}^C \mathbf{x}^C(k) + \mathbf{B}^C \mathbf{v}_t^C(k)) + \frac{w}{2} (\mathbf{A}^C \mathbf{x}^C(k-1) + \mathbf{B}^C \mathbf{v}_t^C(k-1)) = \frac{\mathbf{x}^C(k) - \mathbf{x}^C(k-1)}{\tau}. \quad (\text{B.4})$$

The GENE method requires (B.4) to be rearranged as follows:

$$\mathbf{P}^C \mathbf{x}^C(k) + \mathbf{Q}^C \mathbf{v}_t^C(k) = \boldsymbol{\eta}_x(k).$$

Comparison of this format with (B.4) gives

$$\mathbf{P}^C = \left(\frac{2-w}{2} \mathbf{A}^C - \mathbf{E}_\kappa / \tau \right) \quad (\text{B.5})$$

$$\mathbf{Q}^C = \frac{2-w}{2} \mathbf{B}^C \quad (\text{B.6})$$

$$\boldsymbol{\eta}_x = - \left(\frac{w}{2} \mathbf{A}^C + \mathbf{E}_\kappa / \tau \right) \mathbf{x}^C(k-1) - \frac{w}{2} \mathbf{B}^C \mathbf{v}_t^C(k-1). \quad (\text{B.7})$$

Matrix \mathbf{E}_κ is the identity matrix of dimension κ , where κ is the number of dynamic state variables. The second row of (9) is an algebraic matrix equation and does not require the application of numeric integration.

C. Details of Algorithms in GENE

In Section III, the nodal-analysis-based simulation with GENE is introduced conceptually. In the following, the description is detailed through thorough discussions of the algorithms.

1) *Details of Contractual Interfacing Through Companion Model Emulation:* The Kron reduction formula is applied to eliminate \mathbf{v}_d^C in (7) and obtain the nodal admittance matrix and source vector of the companion model emulation (6) for the child subdivision

$$\mathbf{Y}_N^C = \mathbf{Y}_{tt}^C - \mathbf{T}_{td}^C \mathbf{Y}_{dt}^C \quad (\text{C.8})$$

$$\mathbf{j}_N^C = \mathbf{j}_t^C - \mathbf{T}_{td}^C \mathbf{j}_d^C - \mathbf{Y}_{j_N \mathbf{v}_e}^C \mathbf{v}_e^C \quad (\text{C.9})$$

and the transfer matrices $\mathbf{T}_{td}^C \mathbf{Y}_{j_N \mathbf{v}_e}^C$:

$$\mathbf{T}_{td}^C \mathbf{Y}_{dd}^C = \mathbf{Y}_{td}^C, \quad (\text{C.10})$$

$$\mathbf{Y}_{j_N \mathbf{v}_e}^C = \mathbf{Y}_{te}^C - \mathbf{T}_{td}^C \mathbf{Y}_{de}^C. \quad (\text{C.11})$$

The elements of \mathbf{T}_{td}^C are obtained using forward and backsubstitutions based on the factorization of \mathbf{Y}_{dd}^C into \mathbf{L}_{dd}^C and \mathbf{U}_{dd}^C .

2) *Details of Subdivision Status Indicator and Access Scheme:* The following notation is introduced to detail the status indicator and access scheme:

- ψ number of different types of piecewise linear branch models for which instances exist in a subdivision;
- ν counter which indicates the type of a piecewise linear branch model for which instances exist in the subdivision $\nu \in \{0, \dots, \psi - 1\}$;

- ϕ_ν number of instances of the piecewise linear branch model of type ν in a subdivision $\min \phi_\nu = 1$;
- μ_ν counter which indicates the instance of a piecewise linear branch model $\mu_\nu \in \{0, \dots, \phi_\nu - 1\}$;
- P_ν number of different statuses of the piecewise linear branch model of type ν ;
- $\sigma_{\nu\mu_\nu}$ active status of the instance μ_ν of the piecewise linear branch model of type ν $\sigma_{\nu\mu_\nu} \in \{0, \dots, P_\nu - 1\}$;
- S number of possible status values of a child subdivision;
- s status of a child subdivision $s \in \{0, \dots, S - 1\}$.

For the purpose of illustration, the child subdivision in Fig. 7 with the nonlinearities of the thyristors and saturable smoothing inductor L_{sm} is considered. Let both nonlinear types be modeled through piecewise linear approximations and, therefore, $\psi = 2$. Let the thyristor type be assigned $\nu = 0$ and the saturable smoothing inductor type $\nu = 1$. Then, $\phi_0 = 6$ and $\phi_1 = 1$. The six instances of type $\nu = 0$ are assigned numbers $\mu_0 \in \{0, \dots, 5\}$, and for the one instance of $\nu = 1$, there is only $\mu_1 = 0$. If the thyristor model is represented through two statuses, then $P_0 = 2$. It is reasonable to associate the blocking status of the thyristor model's instance number μ_0 with $\sigma_{0\mu_0} = 0$ and its conducting status with $\sigma_{0\mu_0} = 1$. If the smoothing inductor saturation characteristic is modeled through three different statuses, then $P_1 = 3$ and σ_{10} can adopt three values, i.e., $\sigma_{10} \in \{0, 1, 2\}$.

Through each additional instance of a model of type ν within a subdivision, the total number of possible statuses of this subdivision is multiplied by P_ν . The total number of possible statuses of a child subdivision is thus

$$S = \begin{cases} 1, & \text{for } \psi = 0 \\ \prod_{\nu=0}^{\psi-1} P_\nu^{\phi_\nu}, & \text{for } \psi \geq 1 \end{cases} \quad (\text{C.12})$$

The pseudocode of the algorithm for the calculation of the status of a child subdivision is given in Fig. 14. The status variable s is set to zero at the beginning. Then, a loop that covers all different types of piecewise linear branch models is started. In the mentioned example, these are the types of thyristor and saturable smoothing inductors. Within this loop, a second loop covers all instances of the present type. All of the statuses $\sigma_{\nu\mu_\nu}$ of the instances of piecewise linear branch models are successively polled, multiplied by the factor n , and added to s . The factor n gives the number of different possible statuses due to the ensemble of those piecewise linear branch models which have so far been dealt with by the algorithm. As the algorithm terminates, s gives the status of the subdivision. The functioning can be verified by considering again the example of a subdivision with six instances of the thyristor type and one instance of a saturable smoothing inductor type. For the thyristor type, let instances 1 and 2 be conducting and instances 0, 3, 4, and 5 be blocking. Then, $\sigma_{00} = 0$, $\sigma_{01} = 1$, $\sigma_{02} = 1$, $\sigma_{03} = 0$, $\sigma_{04} = 0$, and

```

n := 1; s := 0
for ν := 0 to ψ - 1 do
  for μν := 0 to φν - 1 do
    s := s + n σν μν
  n := n Pν

```

Fig. 14. Algorithm for the calculation of the status of a child subdivision.

Step 1: Calculate nodal voltages: $\mathbf{Y}_{dd}^c \mathbf{v}_d^c = \mathbf{j}_d^c - \mathbf{Y}_{de}^c \mathbf{v}_e^c - \mathbf{Y}_{dt}^c \mathbf{v}_t^c$.
Step 2: For all branches do: perform branch simulations.
Step 3: According to the status of the subdivision activate prestored \mathbf{Y}_N^c , \mathbf{T}_{td}^c , $\mathbf{Y}_{j_N v_e}^c$, \mathbf{Y}_{de}^c , \mathbf{Y}_{dt}^c , and \mathbf{L}_{dd}^c , \mathbf{U}_{dd}^c in sparse-matrix storage structure.
Step 4: Advance the time dependent excitation sources.
Step 5: According to the sources and the status of the subdivision construct \mathbf{j}_d^c , \mathbf{j}_t^c .
Step 6: Calculate the Norton source: $\mathbf{j}_N^c = \mathbf{j}_t^c - \mathbf{T}_{td}^c \mathbf{j}_d^c - \mathbf{Y}_{j_N v_e}^c \mathbf{v}_e^c$.

Fig. 15. Course of actions in child simulation using GENE.

$\sigma_{05} = 0$. For the one saturable transformer, let $\sigma_{10} = 2$. Then, the status as obtained by the algorithm is

$$s := 2^0 \cdot 0 + 2^1 \cdot 1 + 2^2 \cdot 1 + 2^3 \cdot 0 + 2^4 \cdot 0 + 2^5 \cdot 0 + 2^6 \cdot 2 = 134.$$

Matrices \mathbf{L}_{dd}^c and \mathbf{U}_{dd}^c are calculated and stored in a sparse-matrix storage structure [15] for each status s of a subdivision before the simulation starts. Furthermore, matrices \mathbf{Y}_{de}^c , \mathbf{Y}_{dt}^c , \mathbf{Y}_{td}^c , \mathbf{Y}_{te}^c , and \mathbf{Y}_{tt}^c are constructed for all statuses of the subdivision, and the miniature equivalent matrices \mathbf{Y}_N^c and the associated transfer matrices \mathbf{T}_{td}^c , $\mathbf{Y}_{j_N v_e}^c$ are then calculated using (C.8), (C.10), and (C.11), respectively. For each subdivision status s , the information given through matrices \mathbf{Y}_N^c , \mathbf{T}_{td}^c , $\mathbf{Y}_{j_N v_e}^c$, \mathbf{Y}_{de}^c , \mathbf{Y}_{dt}^c , and \mathbf{L}_{dd}^c , \mathbf{U}_{dd}^c is then stored in fast accessible memory and so rapidly available during the simulation run.

3) *Details of Child Simulation Process:* The pseudocode of the child simulations, which are called in step 2 of the parent simulation process, is given in Fig. 15. Step 1 is concerned with the calculation of the unknown nodal voltages. In step 2, simulations of the branches are performed in the same way as done in Fig. 6 since no further nesting is assumed here within the child simulations. In step 3, refactorizations can be avoided by making use of the subdivision status indicator and access scheme. After advancing the time-dependent excitation sources in step 4, \mathbf{j}_d^c and \mathbf{j}_t^c are constructed in step 5, and the Norton source is calculated in step 6.

Step 6 is performed to provide information to the parent simulation process and, therefore, is different from step 6 of the parent simulation itself. For all other steps, the actions performed at both levels correspond to one another. Differences are mainly concerned with efficiency improvements due to the status indicator and access scheme.

4) *Details of Efficiency Contributions of Subdivision Status Indicator and Access Scheme:* When simulating electromagnetic transients, the computational speed of GENE exceeds the one that is obtained when just using node tearing. This can be recognized by performing an efficiency assessment of the child simulation process for a subdivision with N_d^c dependent nodal voltages and N_t^c terminal nodal voltages. The number of elementary multiplications involved in the matrix operations of the

child simulation process at each time step is counted. No output variables are requested and the initial conditions considered at the branch level are assumed to be known. As a worst-case scenario, it is considered that the matrices are full and that a status change occurs. For the purpose of illustration, passive subdivisions are analyzed, i.e., excitation voltages are only associated with the parent simulation.

Under these assumptions, the solution of the voltages in step 1 of the child simulation in Fig. 15 amounts to $N_d^{c2} + N_d^c N_t^c$ multiplications. In step 6, $N_d^c N_t^c$ multiplications are involved in the calculation of the Norton source. The multiplication count for GENE gives

$$m_{\text{chg}}^{\text{GC}} = N_d^{c2} + 2N_d^c N_t^c.$$

Without the status indicator and access scheme, additional operations need to be performed. The factorization of \mathbf{Y}_{dd}^c into upper and lower triangular matrices takes $(N_d^{c3} - N_d^c)/3$ multiplications. The calculations (C.10) involve $N_d^{c2} N_t^c$ multiplications, and (C.8) is accomplished through $N_d^c N_t^{c2}$ multiplications. The total multiplication count for diakoptics alone then gives

$$m_{\text{chg}}^{\text{DC}} = \left(N_d^{c3} - N_d^c \right) / 3 + N_d^{c2} + N_d^c N_t^c + N_d^c N_t^{c2} + 2N_d^c N_t^c.$$

When factorizations are to be performed as a result of status changes, the number of multiplications rises with the cube of the number of nodes with unknown nodal voltages, i.e., with N_d^{c3} in the count of $m_{\text{chg}}^{\text{DC}}$. This is not the case for GENE as evidenced by $m_{\text{chg}}^{\text{GC}}$. In fact, in GENE, the multiplication count does not change with status changes but remains constant. This makes the method suitable for real-time applications where a constant computational effort at any time step is desired.

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